

1 Teresa M. Corbin (SBN 132360)
Denise M. De Mory (SBN 168076)
2 Jaclyn C. Fink (SBN 217913)
HOWREY LLP
3 525 Market Street, Suite 3600
San Francisco, California 94105
4 Telephone: (415) 848-4900
Facsimile: (415) 848-4999
5
6 Attorneys for Plaintiff SYNOPSYS, INC.
and for Defendants AEROFLEX INCORPORATED,
AMI SEMICONDUCTOR, INC., MATROX
7 ELECTRONIC SYSTEMS, LTD., MATROX
GRAPHICS, INC., MATROX INTERNATIONAL
8 CORP., MATROX TECH, INC., and
AEROFLEX COLORADO SPRINGS, INC.
9

10 UNITED STATES DISTRICT COURT
11 NORTHERN DISTRICT OF CALIFORNIA
12 SAN FRANCISCO DIVISION
13

14 RICOH COMPANY, LTD.,

15 Plaintiff,

16 vs.

17 AEROFLEX INCORPORATED, AMI
SEMICONDUCTOR, INC., MATROX
18 ELECTRONIC SYSTEMS LTD., MATROX
GRAPHICS INC., MATROX
INTERNATIONAL CORP., MATROX TECH,
19 INC., AND AEROFLEX COLORADO
SPRINGS, INC.
20

21 Defendants.
22

23 SYNOPSYS, INC.,

24 Plaintiff,

25 vs.

26 RICOH COMPANY, LTD.,

27 Defendant.
28

Case No. C03-04669 MJJ (EMC)

Case No. C03-02289 MJJ (EMC)

**NOTICE OF MOTION AND MOTION FOR
SUMMARY JUDGMENT OF INVALIDITY
OF CLAIMS 13-17 OF U.S. PATENT NO.
4,922,432**

[Dispositive Motion No. _4]

Date: September 26, 2006
Time: 9:30 a.m.
Courtroom: 11, 19th Floor
Judge: Martin J. Jenkins

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1 PLEASE TAKE NOTICE that on September 26, 2006, at 9:30 a.m., before the Honorable
2 Martin J. Jenkins in Courtroom 11, 19th Floor, in the United States District Court, 450 Golden Gate
3 Avenue, San Francisco, California, Plaintiff Synopsys, Inc. (“Synopsys”) and Defendants Aeroflex
4 Incorporated, Aeroflex Colorado Springs, Inc., AMI Semiconductor, Inc., Matrox Electronic Systems
5 Ltd., Matrox Graphics Inc., Matrox International Corp., and Matrox Tech, Inc. (“the Customer
6 Defendants”) will move for summary judgment pursuant to Rule 56 of the Federal Rules of Civil
7 Procedure that claims 13-17 of the patent-in-suit, U.S. Patent No. 4,922,432 (the “’432 patent”) is
8 invalid for failure to comply with the statutory requirements of 35 U.S.C. §§ 102, 103, and 112.

9 This motion is based on the memorandum of points and authorities set forth below, the
10 accompanying declarations, exhibits, and proposed order, any argument of counsel at the hearing on
11 this motion, and all other pleadings and matters of record in these actions.

12 I. INTRODUCTION

13 It is axiomatic that, in order to be valid, a patent must be novel and nonobvious. That is, a
14 patent must be a true invention, not just a retread of what someone else previously created, or such a
15 small variant from what preceded it that any person of skill in the art would have been able to create it
16 from the prior art. Unfortunately for Ricoh, that is precisely the case with the ’432 patent. Claims 13-
17 17 — the only asserted claims — never should have issued. The “invention” described in these claims
18 was entirely anticipated (or, at the least, rendered obvious) by myriad references published more than
19 one year prior to the January 13, 1988 filing date of the patent. These facts invalidate Claims 13-17 of
20 the patent, and Defendants seek an order granting them summary judgment of invalidity of the ’432
21 patent.

22 Claims 15 and 17 are invalid for the additional reason that they do not claim any further
23 limitation beyond their parent claim. This is a violation of § 112 ¶ 4, and requires the invalidation of
24 these claims.

25 II. STATEMENT OF FACTS

26 Although there are many prior art references that anticipate the ’432 patent, to simplify this
27 motion, Defendants move only on the Kowalski/VDAA references. Below, we present the basic
28 elements of the asserted claims of the ’432 patent, and the Kowalski/VDAA prior art.

A. The invention described in Claims 13-17 of the '432 patent.

The '432 patent issued on May 1, 1990 out of an application filed on January 13, 1988. As the Court is aware, the '432 patent describes a synthesis tool — that is, a computer program that takes an architecture independent description of the functionality of an integrated circuit and transforms that description into a gate-level netlist. Although Ricoh has continually trumpeted in this litigation its “invention,” there is absolutely no allegation in this case (or could there be) that Ricoh’s '432 patent is a pioneer invention — i.e., the first ever synthesis tool. Indeed, Ricoh has stated that the only alleged inventive aspect in the '432 patent is the “unique combination” of elements. Thus, the elements and their flow is critical to understanding the alleged invention and determining whether it was anticipated.

There are six elements in independent claim 13, designated below by letters:

A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising:
 [A] storing a set of definitions of architecture independent actions and conditions;
 [B] storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set;
 [C] storing in an expert system knowledge base a set of a rules for selecting hardware cells to perform the actions and conditions;
 [D] describing for a proposed application specific integrated circuit a series of architecture independent actions conditions;
 [E] specifying for each described action and condition of the series of one of said stored definitions which corresponds to the desired action or condition to be performed; and
 [F] selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.

The six steps in Claim 13 describe a fairly simple process. First, elements A, B, and C are stored to be available for use later. In element D, the ASIC is described in a series of architecture independent actions and conditions, element E takes the described actions and conditions, and specifies a definition for each input action or condition from the definitions stored in element A. In element F, cell selection rules are applied to the output of Element E (the specified definitions) to select hardware

cells contained in element B and a netlist is generated. A very simplified flow of the claimed process is thus:

Store: Defintions Data describing hardware cells Cell election rules
Describe ASIC using a series of actions and conditions
Specify a stored definition for each action and condition
Select stored cells by applying stored cell selection rules to stored specified definitions and generate a netlist of hardware cells and interconnections

Independent Claims 14-17 each purport to add an additional step to the above process. Claim 14 adds the step of generating mask data. Claim 15 adds the step of generating data paths, whereas Claim 16 adds the step of generating these data paths through rules stored in a knowledge base. Claim 17 adds the step of generating control paths.

B. Claim construction of terms.

The Court has construed many of the terms used in the patent. Ex. 8.¹ This construction is, of course, what the attached claim charts are based upon. However, the Court has not construed the term

¹ Unless otherwise noted, all exhibits referenced in this motion are attached to the Declaration of Denise M. De Mory In Support of Synopsys' and Customer Defendants' Summary Judgment Motions filed concurrently herewith. All deposition references are likewise included in the De Mory Declaration.

1 “hardware cells.” As Synopsys and the Customer Defendants have explained elsewhere (*see* Summary
 2 Judgment Motion No. 2), the plain meaning of “hardware cell” is a cell that maps or corresponds to a
 3 specified function from element E. In words, if the definition specified in element e is “add” then the
 4 selected hardware cell must be an implementation of an adder, and not as Ricoh contends, primitive
 5 logic gates, such as AND, OR, NOR (as Ricoh claims) For purposes of this motion, Synopsys and the
 6 Customer Defendants utilize the same definition of “hardware cells” that they do in their non-
 7 infringement motion, and defer largely to the explanation set forth in that motion.

8 The Defendants asserted during claim construction that the term “netlist” in claim 13 should be
 9 construed as including “the necessary control and data path information for connecting the hardware
 10 cells and the controller” based on the ’432 patent’s specification and the embodiment disclosed. Ex.
 11 34, Exh. A at 19 (clause “P”).² Ricoh argued that Defendants’ construction was too narrow, and the
 12 Court agreed, defining the phrase “a netlist defining the hardware cells which are needed to perform
 13 the desired function of the integrated circuit” as “a description of the hardware components (and their
 14 interconnections) needed to manufacture the ASIC as used by subsequent process, e.g., mask
 15 development, foundry, etc.” Ex.8 at 24. The Court specifically noted that “claim 13 does not *restrict*
 16 the interconnection requirements of the hardware cells to ‘data and control paths,’” implying that the
 17 interconnections the Court was referring to in its construction *does* include data and control paths. *Id.*
 18 (emphasis added)

19 C. The Kowalski references and the VDAA system.

20 In April 1984, a Ph.D. student at Carnegie Mellon University, Thaddeus J. Kowalski, wrote his
 21 dissertation on a synthesis tool he dubbed the VLSI Design Automation Assistant (“VDAA”).³ Ex. 35.
 22 (“Kowalski Thesis”). Dr. Kowalski published several papers on his VDAA program, including a short
 23
 24

25 ² Unless otherwise noted, all exhibits referenced in this motion are attached to the Declaration of Denise M. De Mory In
 26 Support of Synopsys’ and Customer Defendants’ Summary Judgment Motions filed concurrently herewith. All deposition
 references are likewise included in the De Mory Declaration.

27 ³ Although Dr. Kowalski referred to the system as “DAA,” we refer to it as “VDAA” to differentiate this system from a
 28 completely different system developed at CMU in the 1970’s known as CMU/DA.

1 article in August 1985 titled “The VLSI Design Automation Assistant: From Algorithms to Silicon.”
2 Ex. 36 (“Kowalski85”).

3 As described in detail in the claim charts attached hereto as Exhibits A and B, the Kowalski
4 Thesis and Kowalski85 fully anticipate claims 13-17 of the ’432 patent. The VDAA system accepted
5 as input an algorithmic description of the behavior of the chip, written in a language known as ISPS,
6 and the ISPS description described the desired functionality of the chip in terms of actions and
7 conditions. Ex. 35 at 46-47. Thus, element D is met, because the circuit is described.

8 This ISPS description was then translated into a data-flow graph representation known as VT
9 by the VDAA system. In the process of compiling the design into a VT, the compiler translated each
10 of the actions and conditions into a predefined operator, which forms the node of the graph. Ex. 35 at
11 49. Thus, both elements A and E are met — the operators are the “definitions of the architecture
12 independent actions and conditions,” they were predefined (“stored” as required by element A), and
13 specified (assigned to a stored definition as required by element E).

14 From there, the nodes in the VT representation were used to select hardware cells from the
15 “technology-sensitive database” using expert rules stored in the VDAA system. *Id.* The rules were in
16 an IF-THEN antecedent format. *Id.* Thus, the stored rules (element C) were used to select the stored
17 hardware cells (element B). After the hardware cells were bound using the module binder, a netlist
18 was created by the control allocator. *Id.* Thus, element F is satisfied.

19 At deposition, Dr. Kowalski clarified that the “technology sensitive” database discussed in
20 these papers contained cell descriptions that “could be as low as a single an[d] gate or as high and
21 complicated as an ALU.” Ex. 37(Kowalski) at 83:11-24.

22 In addition to his affiliation with CMU, Dr. Kowalski was a researcher at AT&T Bell
23 Laboratories, and after receiving his doctorate in 1984 for his work on VDAA, Dr. Kowalski further
24 refined the program at AT&T. Ex. 37 (Kowalski) at 103:17-104:6. One of these refinements was to
25 eliminate the need for a separate module binder process — the hardware cells were selected, bound,
26 and a netlist was created all in one step. Ex. 37 (Kowalski) at 104:8-25; 117:4-10; 118:7-119:12. This
27 revised VDAA system is described in the claim chart attached hereto as Exhibit C.

28

1 Recently, an anonymous requestor asked for the '432 patent to be reexamined by the USPTO in
 2 light of the Kowalski Thesis and Kowalski 85. Ex. 38. The PTO granted this request, and the '432
 3 patent is in reexamination on the basis of these two references. Ex. 39. The PTO noted that the
 4 Kowalski references, both individually, together, and in combination with other references, raised
 5 substantial new questions of patentability. No office action has yet issued from this reexamination.

6 **III. ARGUMENT**

7 As demonstrated by the attached claim charts, the various Kowalski/VDAA references are
 8 anticipatory. In addition, claims 15 and 17 are invalid on a separate basis — for failure to add
 9 limitations beyond those of the parent claim.

10 **A. Legal standards.**

11 The Patent Act states that a person is not entitled to a patent if “the invention was patented or
 12 described in a printed publication in this or a foreign country or in public use or on sale in this country,
 13 more than one year prior to the date of the application for patent in the United States.” 35 U.S.C.
 14 § 102 (b). This section is known as a statutory bar, and it absolutely bars the obtaining of a patent on
 15 an invention that was (1) publicly used or on sale more the one year prior to the filing date of the
 16 patent or (2) disclosed in any prior publication that anticipates the claims or renders them obvious.
 17 *See Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1568 (Fed. Cir. 1988) (affirming
 18 invalidity of two patents under § 102(b) and describing the section as a “statutory bar via prior
 19 description, use, or being on sale.”).

20 Under § 102(b), a device qualifies as prior art if it was in public use more than one year prior to
 21 the date of the patent. 35 U.S.C. § 102. An invention is in public use “where it is exposed or
 22 demonstrated to persons other than the inventor ... who are under no obligation of secrecy.” *Nordberg,*
 23 *Inc. v. Telsmith, Inc.*, 882 F. Supp. 1252, 1283 (E.D. Wis. 1995), *aff’d*, 82 F.3d 394 (Fed. Cir. 1996).
 24 “Use of a single specimen, even in a factory and in the presence only of the employees, may be
 25 “public” use under certain circumstances.” *Id.* at 1284 (citation omitted). Further, a public use “means
 26 the dissemination of an idea without substantive restriction.” *AMP, Inc. v. Fujitsu Microelectronics,*
 27 *Inc.*, 853 F. supp. 808, 816 (M.D. Pa. 1994) (citation omitted).

1 When challenging the validity of an issued patent, the moving party must demonstrate
 2 invalidity by clear and convincing evidence. *See Enzo Biochem, Inc. v. Gen-Probe, Inc.*, 424 F.3d
 3 1276, 1281 (Fed. Cir. 2005). Despite this standard, summary judgment under the statutory bar is
 4 appropriate when there is no material issue of fact that a reference published, used, or sold more than a
 5 year prior to the filing date anticipates or renders obvious a claim. *Telemac Cellular Corp. v. Topp*
 6 *Telecom, Inc.*, 247 F.3d 1316, 1330 (Fed. Cir. 2001) (affirming summary judgment of invalidity of
 7 patent in light of anticipating prior publication).

8 In general, summary judgment is granted to a moving party when “there is no genuine issue as
 9 to any material fact” and the “moving party is entitled to judgment as a matter of law.” FED. R. CIV. P.
 10 56(c). Summary judgment is just as reasonable in a patent case as in any other case. *See Barmag*
 11 *Barmer Maschinenfabrik AG v. Murata Mach., Ltd.*, 731 F.2d 831, 835 (Fed. Cir. 1984). Although
 12 anticipation under § 102(b) is a question of fact, it still may be decided on summary judgment.
 13 *Telemac*, 247 F.3d at 1327. Moreover, “[s]ummary judgment is not a disfavored procedural shortcut,
 14 but rather an essential thread in the fabric of the Federal Rules that eliminates unfounded claims
 15 without recourse to a costly and lengthy trial.” *Colgate Palmolive Co. v. W.L. Gore & Assoc., Inc.*,
 16 919 F. Supp. 767, 769 (D.N.J. 1996). Once a party has made an initial showing that summary
 17 judgment is warranted, the opposing party may not rest upon pleadings; rather, “the non-moving party
 18 must ‘designate specific facts showing that there is a genuine issue for trial.’” *Tinoco v. Belshe*, 916 F.
 19 Supp. 974, 979 (N.D. Cal. 1995) (quoting *Celotex Corp. v. Catrett*, 477 U.S. 317, 324 (1986)). The
 20 Court may grant summary judgment if Ricoh’s evidence “is merely colorable, or is not significantly
 21 probative.” *Tinoco*, 916 F. Supp. at 979 (quoting *Anderson v. Liberty Lobby*, 477 U.S. 242, 249-250
 22 (1986)).

23 **B. The Kowalski/VDAA references anticipate Claims 13-17.**

24 The Kowalski Thesis and Kowalski 85 reference are both printed publications dated prior to the
 25 critical date of January 13, 1987, with publication dates of 1984 and 1985, as noted on the cover pages
 26 of the two references. Exs. 35 and 36. Thus, these two references qualify as potential § 102(b) art.
 27 Furthermore, they, along with deposition testimony from Dr. Kowalski, describe a working system
 28

1 which was in public use in the United States more than a year prior to the filing of the patent, so the
2 VDAA system is itself potential § 102(b) art.

3 Each of these references — the papers and the system itself (in its various versions) —
4 anticipate Claims 13-17 of the '432 patent, as shown in the attached claim charts. As the charts
5 demonstrate, the references describe a synthesis tool which takes as input a behavioral description of a
6 chip, translates that input using a stored set of definitions, and uses the translated input, a set of stored
7 hardware cells (“modules”) and a set of expert rules to select cells and create a netlist. These charts
8 suffice to shoulder the Defendants’ burden of proving invalidity by clear and convincing evidence.

9 **1. The references are anticipatory under Synopsys’ and the Customer**
10 **Defendants’ definition of “hardware cell.”**

11 When properly considered, there is only a very limited dispute about whether or not VDAA
12 anticipates the asserted claims, and that relates solely to the definition of “hardware cell.” Dr.
13 Soderman, Ricoh’s expert, claims three elements are missing from the Kowalski references and
14 VDAA: the stored hardware cells, the expert rules to select hardware cells, and the netlist of selected
15 hardware cells. These assertions depend entirely on whether or not Ricoh is right on its construction of
16 “hardware cell.” Clearly, VDAA uses rules to select modules corresponding to the functions (i.e.,
17 specified definitions). This can only fail to meet the claims if Ricoh is correct that rules must be used
18 to select cells consisting solely of primitive gates. Ricoh is not correct.⁴

19 The language of the first part of the selection step is: “selecting from said stored data [the
20 hardware cell data stored in element B] for each of the specified definitions [specified in element E] a
21 **corresponding integrated circuit hardware cell.**” The Court interpreted this language to require
22 “mapping the specified stored function to a corresponding stored hardware cell.” Ex. 8 at 20.
23 Synopsys and the Customer Defendants claim that, in accordance with the language of the claim, as
24 well as the Court’s clear construction of the claim language, what occurs in this step is that the
25

26
27 ⁴ Synopsys’ and the Customer Defendants’ full claim construction argument on “hardware cell” is spelled out in Summary
28 Judgment No. 2.

1 specified function is being assigned to a “hardware cell.”⁵ In other words, if the specified definition is
 2 “ADD (A,B,C),” which is an exemplary macro in the ‘432 patent specification, the only type of
 3 hardware cell to which the function ADD can be mapped is an adder. Put another way, the only
 4 “hardware cell” that corresponds to the function add is an adder. This is the only way that the patent
 5 claim makes sense, and this interpretation is consistent with the specification.

6 The portion of the claim after the comprising step further confirms that the hardware cells need
 7 not be individual gates. The claim requires that the selection process be “comprised of” a two step
 8 process: (1) “**applying to the specified definition** of the action or condition to be performed, **a set of**
 9 **cell selection rules stored** in said expert system knowledge base” and (2) “generating for the selected
 10 integrated circuit hardware cells, a netlist defining the hardware cells . . .” In other words, the patent
 11 requires that “hardware cells” corresponding to the specified definitions be selected by applying rules
 12 to those definitions, and that, *subsequently*, a netlist be generated “defining” the selected integrated
 13 circuit hardware cells.⁶ Ex. 1 at 16:61-62. Thus, the first step is applying the rules to the definitions to
 14 select the hardware cells, which in the case of VDAA is, as described above, applying the rules to the
 15 operators to select the modules. The second step, generating for the selected integrated circuit
 16 hardware cells (confirming that the cells were selected in the prior step), a netlist, defining (not
 17 comprised of or listing) the hardware cells is likewise practiced by VDAA, occurring during module
 18 binding when the actual netlist is generated.

19 In view of the foregoing, there is no doubt that the VDAA system practices this method via the
 20 selection of technology dependent modules by applying rules to the operators in the VT. Specifically,
 21 the VDAA, a knowledge based-expert system, applies a set of rules to each of the definitions to select
 22 a module. The VDAA modules are “hardware cells,” and these modules are selected by rules.

24 ⁵ Indeed, the Court’s claim construction interprets this element to mean exactly what Synopsys and Customer Defendants
 25 contend: “mapping the specified function to a corresponding hardware cell.” Claim Construction Order at 20.

26 ⁶ This also is fully consistent with the patent’s specification. The specification says “the netlist is generated after the cells
 27 have been selected by the PCSC.” Col. 9:64-65. The specification goes on to explain the information that is used in netlist
 28 generation which include the information in the cell library, which is comprised of for each hardware cell (also called a
 block), the following information: type out: Col. 9:24-50. Given that the cell library included transistor level descriptions
 as well as mask data, a netlist as well as mask data could readily be generated.

1 Subsequent to that selection, a netlist is generated for these cells in the module binder. Nothing more
2 is necessary, and the Kowalski/VDAA references anticipate the '432 patent. Because Dr. Soderman's
3 and Ricoh's position on this issue is flawed as a matter of law, summary judgment should be granted
4 that the VDAA anticipates claim 13.

5 **2. The references are anticipatory even under Ricoh's flawed definition of**
6 **"hardware cell."**

7 Even if there were a requirement that the "hardware cells" of the patent claim be individual
8 gates (as opposed to representations of circuit components), the original VDAA described in the papers
9 meet that requirement. Dr. Kowalski testified that the "technology sensitive database" had cell
10 descriptions, which *included* single gates as well as more complicated structures such as ALUs. Ex. 37
11 (Kowalski) at 83:5-24. Thus, the VDAA system, which was in public use more than a year prior to the
12 filing of the patent application, did store individual gates and had those gates selected by expert rules,
13 meeting the "hardware cell" limitations even under Ricoh's definition.

14 Furthermore, the version of VDAA created by Dr. Kowalski at Bell Labs by 1985 also clearly
15 met Ricoh's requirement that there be direct selection of gates by rules. In the later version of VDAA,
16 created in 1985, Dr. Kowalski incorporated the module binder into the cell selection process. Ex. 37
17 (Kowalski) at 14:4-16; 17:6-19:7; 125:2-10. This incorporated module binder, called Fred, used the
18 expert rules contained in the VDAA system to choose *and bind* the modules in one step. Ex. 37
19 (Kowalski) at 116:22-119:9; 127:14-128:6. Even though this version of the VDAA system was never
20 reported via a journal article, the fact is that this version of VDAA existed, and Ricoh cannot seriously
21 dispute that it did exist. It was in public use, because AT&T directed Dr. Kowalski, instead of
22 patenting the system, to "publish widely and place the work in the public domain." Ex. 37 (Kowalski)
23 at 21:6-7. In these circumstances, the version of VDAA created at AT&T was in public use in the
24 United States in 1985, more than one year prior to Ricoh filing of the application for the '432 patent,
25 and is therefore invalidating prior art under § 102(b).

C. Claims 15 and 17 do not add additional limitations to Claim 13 and are therefore invalid.

Claim 13 sets forth a clear methodology, as described above. At the end of the process, a netlist is generated. According to the construction given by the Court, this netlist contains all “hardware components (and their interconnections) needed to manufacture the ASIC....” This necessarily means that the netlist includes data paths and control paths, and thus requires that the data paths and control paths be generated prior to the netlist generation claimed in claim 13.

There is one odd thing about this observation. Claims 15 and 17 each purport to add “the further step” of generating data paths (claim 15) and control paths (claim 17) to claim 13. But because claim 13 already includes these steps, dependent claims 15 and 17 are superfluous and add no further limitation to claim 13.⁷

Given this analysis, claims 15 and 17 are invalid because they do not comply with the statutory requirements of 35 U.S.C. § 112, ¶ 4. Section 112, ¶ 4 requires “a claim in dependent form shall ... specify a further limitation of the subject matter claimed.” *See Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1381 (Fed. Cir. 1988). In *Curtiss-Wright*, the Federal Circuit reasoned that “reading an additional limitation from a dependent claim into an independent claim would not only make that additional limitation superfluous, it might render the dependent claim invalid” under 35 U.S.C. § 112, ¶ 4. *Id.* at 1380. The Federal Circuit in *Pfizer, Inc. v. Ranbaxy Labs. Ltd.* recently confirmed the reasoning of the *Curtiss-Wright* opinion when it held a claim invalid for failing to comply with § 112, ¶4. 2006 U.S. App. LEXIS 19416 *19 (Fed. Cir. Aug. 2, 2006). The Federal Circuit properly recognized that it “should not rewrite claims to preserve validity.” *Id.* at *18 (citation omitted). “If the only claim construction that is consistent with the claim’s language and the written

⁷ The claim construction doctrine of claim differentiation does not change this result. Claim differentiation merely creates a *presumption* that dependent claims are of different scope than their parent claims; it does not mandate such a result. *Seachange Int’l v. C-COR, Inc.*, 413 F.3d 1361, 1369 (Fed. Cir. 2005) (claim differentiation “presumption is not a hard and fast rule and will be overcome by a contrary construction dictated by the written description or prosecution history”) (citation omitted). Where both parties agreed, and the Court found, that the proper construction of the term “netlist” in Claim 13 requires that a netlist contain, as interconnections, (at the very least) data paths and control paths, the presumption has already been overcome.

1 description renders the claim invalid, then ... the claim is simply invalid.” *Id.* at *18-19. Because
2 claim 13 implicitly includes the steps of generating data paths and control paths, claims 15 and 17
3 should be invalidated under § 112, ¶ 4, for failure to recite a further limitation to their parent claim.

4 **IV. CONCLUSION**

5 For the foregoing reasons, Defendants respectfully request that the Court grant their motion and
6 issue a summary judgment of invalidity of the ’432 patent.

7 Dated: August 18, 2006

HOWREY LLP

9 By: _____

10 Denise M. De Mory
11 Attorney for Plaintiff SYNOPSYS, INC.
12 and Defendants AEROFLEX
13 INCORPORATED, AMI
14 SEMICONDUCTOR, INC., MATROX
15 ELECTRONIC SYSTEMS, LTD.,
16 MATROX GRAPHICS INC., MATROX
17 INTERNATIONAL CORP., MATROX
18 TECH, INC., and AEROFLEX
19 COLORADO SPRINGS, INC.